4638494) or Abrahamson et al. (5022049). In addition, the drawings were also objected to because they lack formality and clarity. Replacement drawings containing no new matter, and in accordance with 37 C.F.R 1.121(d), are enclosed herein. The Examiner is requested to reconsider the rejection claims in light of the reasoning presented below. A separate sheet showing the status of all claims, in accordance with C.F.R. 121 is enclosed.

First it will be appreciated that Ogawa is using Gold Codes. It will be further appreciated that Gold Codes are generated by modulo-2 *addition of two maximal* sequences with *the same length*. The code sequences are added chip by chip by synchronous clocking. Stated differently *Gold codes* are all about *combining equal-length m sequence codes* to form large numbers of orthogonal codes. The generated Gold codes are of the same length as the two m sequences. Nowhere does Ogawa disclose or suggest relatively prime component codes so that the composite code length is the *product of the length of the prime component codes* (Lxyz = Lx times Ly times Lz). Indeed, *Ogawa teaches away from relative prime code generation* since all of Ogawa's pictures *disclose equal-length code generators*.

In the claim by claim analysis below it will be shown that the present application claims features not otherwise disclosed or suggested by the prior art.

102(b) rejections

Claims 1-18 and 22-23 are pending in this case. Claims 1-5, 9-12, 22, and 23 were rejected under 35 U.S.C. 102(b) as being anticipated by Ogawa et al. (US2002/0181558).

Claim 1 of the present application recites the features of a receiver logic combiner adapted to generate a plurality of *relatively prime composite PN codes*, wherein *each* of the plurality of composite PN codes *are separated by a predetermined PN phase.* (Claim 1 has been amended herein to more distinctly reveal this feature.)

Ogawa, on the other hand, *does not disclose or suggest generating PN codes which are relatively prime*, i.e., the component codes are each different prime number lengths. As pointed out above and repeated here, *Ogawa teaches away* from component codes of different lengths. (Ogawa Figures 4-6 and 8-16). It will also be appreciated that *Ogawa's exclusive-or* function defines that the resulting composite code must be the same length as the two input codes and that each of the two input codes are also identical length codes, e.g., *m*-sequence codes. (Ogawa paragraphs 17, and 59-71) In other words Ogawa does not, and cannot, disclose or suggest the feature of relatively prime PN codes *wherein the code components are of different prime lengths as recited in the present application*.

As pointed out above and repeated here, Claim 1 of the present application also recites the feature of the *composite* PN codes are *separated by a predetermined PN phase.*

Ogawa, by comparison, is just using different phases of *equal-length codes* to generate different and orthogonal *m-length Gold Codes*. Ogawa does not delay the output of one generator by one, two, or any number of chips to generate a different phase of the *composite PN code* as recited in the present application. Nothing from Ogawa discloses or suggests phase shifting by delaying the output of one component generator by

one or more chips. Ogawa's figure 12 almost looks like it, but the outputs (35, 36, and 37) are linear feedback shift registers and not delays. Thus, Ogawa neither discloses or suggest all the features recited in Claim 1 of the present application.

Claim 2 of the present application recites the features of at least three first receiver pseudo-noise (PN) component code generators wherein each of the generators generate *relatively prime PN component codes.* Nowhere does Ogawa disclose or suggest relatively prime PN codes.

Claim 3 of the present application rises or falls with Claim 2.

Claim 4 of the present application rises or falls with Claim 2.

Claim 5 of the present application recites the feature wherein the predetermined PN phase substantially equals at least one PN minor epoch. Ogawa's delay, on the other hand, merely rotates or slips a code one phase (state or tap) at a time so that it appears like a different code to be added to form another m-length Gold Code. Ogawa's delay is not disclosed as deterministic. Ogawa's phase may be predetermined, i.e., selecting an output from a shift register stage corresponding to some delay (Figs 2A, 5, and para. 59) but the amount of phase shift to the COMPOSITE code is not disclosed as deterministic. In the present application, the COMPOSITE code phase shift, effected by delaying the phase of one component

code by one chip, is deterministic. Delay one component code 1 chip, and the phase shift experienced by the COMPOSITE code is substantially a phase offset in the COMPOSITE code equal to at least one combination epoch of the component codes not slipped. The COMPOSITE code slip is a number (many) times the lengths of the component codes not experiencing the one or more chip delay relative to the other component codes. Thus, the PN COMPOSITE code phase can be determined in accordance with features of the present invention. Claim 5 has been amended herein to more clearly reveal these features.

Nowhere does Ogawa distinguish between component and COMPOSITE codes and nowhere does Ogawa disclose or suggest a delay substantially equaling at least one combination epoch of component codes not slipped.

Claim 9 of the present application recites the features of generating a first composite PN code; and generating a second composite PN code, wherein the second composite PN code is PN phase separated from the first composite PN code. In other words, the phase separation is a predetermined phase separation. *Nowhere does Ogawa disclose or suggest predetermined phase separation between relatively prime composite codes.*

Claim 10 of the present application recites the features of generating a plurality of *relatively prime PN component codes*; PN phase delaying one of the plurality of relatively prime PN component codes; and combining the plurality of relatively prime PN component codes. As pointed out above and repeated here, nowhere does Ogawa disclose or suggest relatively prime PN component codes. Also pointed out earlier, *Ogawa teaches*

away from generating relatively prime PN component codes in that Ogawa teaches the use of GOLD codes with identical length *m*-sequence codes.

Claim 11 of the present application recites the features of generating the plurality of relatively prime PN component codes; and combining the plurality of relatively prime PN component codes. Nowhere does Ogawa disclose or suggest relatively prime PN codes.

Claim 12 of the present application recites the feature of generating a second composite PN code at least one PN minor epoch phase separated from the first composite PN code. Ogawa's delay, on the other hand, merely rotates or slips a code one phase (state or tap) at a time so that it appears like a different code to be added to form another m-length Gold Code. Ogawa's delay is not disclosed as deterministic. Ogawa's phase may be predetermined, i.e., selecting an output from a shift register stage corresponding to some delay (Figs 2A, 5, and para. 59) but the amount of phase shift to the composite code is not disclosed as deterministic. In the present application, the component code phase shift, effected by delaying the phase of one component code by one chip, is deterministic. Delay one component code 1 chip, and the phase shift experienced by the composite code is *substantially equal to at least one combination epoch of the component codes not slipped*. Nowhere does Ogawa distinguish between component and COMPOSITE codes and nowhere does Ogawa disclose or suggest a delay substantially equaling at least one combination epoch of component codes not slipped. Claim 12 has been amended herein to more clearly reveal these features.

Claim 22 of the present application recites the feature of a program of instructions executable by the machine to perform method steps for generating multi-phase composite pseudo-noise (PN) codes. In addition, Claim 22 recites the features of generating a plurality of *relatively prime PN component* codes and combining the plurality of relatively prime PN component codes to generate a composite PN code. Claim 22 also recites the feature of generating a second plurality of *relatively prime PN component* codes, wherein one of the component codes is PN phase delayed, and combining the plurality of relatively prime PN component codes to generate a second composite PN code. The result is that *the second composite PN code is phased delayed by a deterministic delay substantially equal to at least one combination epoch of the component codes not slipped*. Nowhere does Ogawa disclose or suggest phase delaying a component code by a predetermined phase delay, i.e., PN phase delay, to form a second composite PN code phased delayed where the phase delay is substantially equal to at least one combination epoch of component codes not slipped.

Claim 23 of the present application recites a program storage device having at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file. Nowhere does Ogawa disclose or suggest VHDL language files.

103(a) rejections

Claims 6-8 and 13-18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. in view of Kartchner et al. (US 4638494) or Abrahamson et al. (5022049).

Dependent claims 6-8, and 13-18 all recite the features of MAND, MAJ, or MOD logic combination of the relatively prime PN codes. As pointed out earlier and repeated here Ogawa fails to disclose or suggest the parent claim features of *predetermined phase separation between relatively prime composite codes* from which these claims depend. In addition, neither does Kartchner et al., or Abrahamsom et al., disclose or suggest MAND, MAJ, or MOD logic combination of the relatively prime PN codes where one of the combination codes has been PN phased delayed by a predetermined amount.

The Applicants respectfully assert that all of the pending claims are now in a condition for allowance.

Filed concurrently within PAIR is the fee for a petition for a one month extension of time.

Should any unresolved issue remain, the Examiner is invited to call Applicant's Attorney at the telephone number indicated below.

Respectfully submitted,

/Kevin P. Correll/	01/06/08
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